ATLAS Upgrade

- from a TileCal perspective

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On behalf of the ATLAS collaboration

Overview

Introduction
Phase 1
Phase 2
Summary

The presentation is to a large extent based on slides from colleagues

Current Status

LHC designed for $10^{34}cm^{-2}s^{-1}$ @ 7+7 TeV
Limited to 3.5+3.5 TeV due to magnet problems – otherwise runs well
Should reach $10^{34}cm^{-2}s^{-1}$ and 7+7 TeV (6.5+6.5 TeV) after two years of magnet consolidation

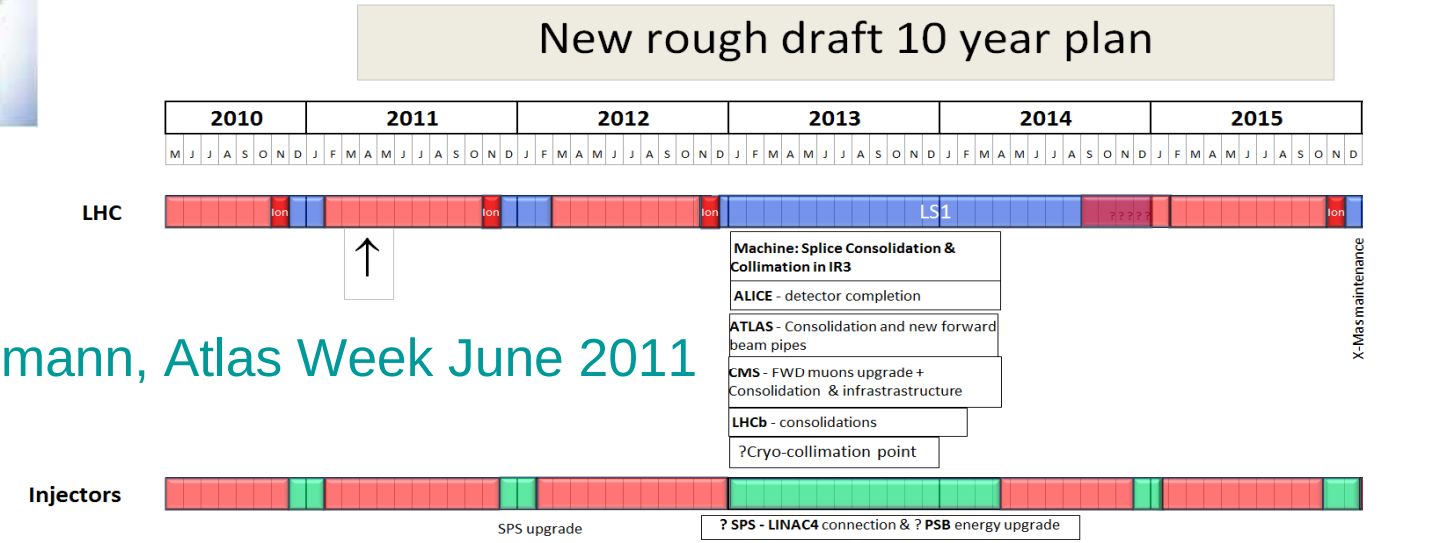
ATLAS also runs well – some consolidation needed

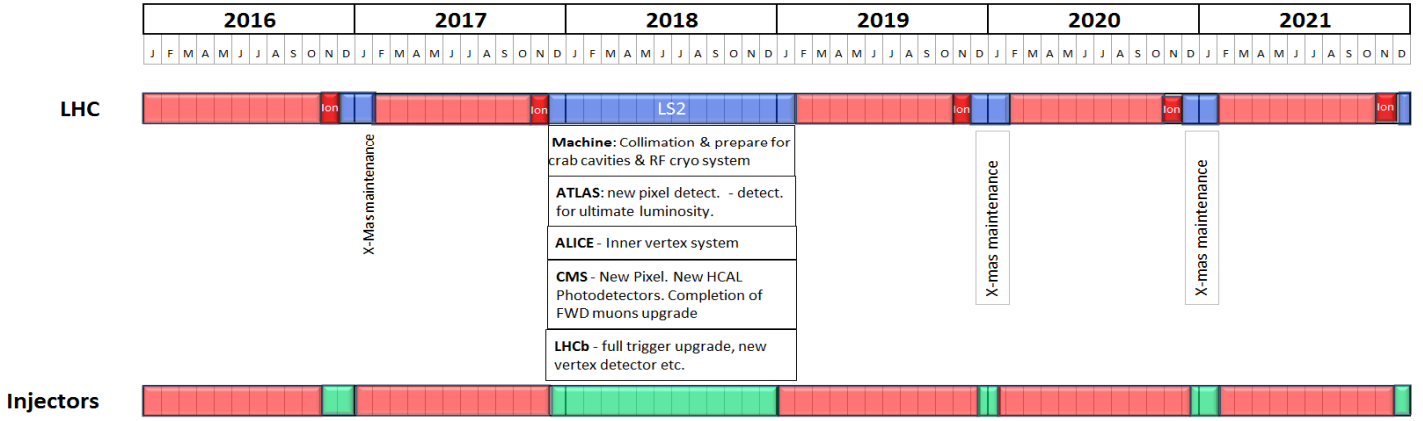
Why upgrade?

Adapt to improved LHC luminosity – factor 10 possible
Adapt to changing physics requirements
Remember that much must be replaced anyway due to old age and radiation damage

Current (not yet approved)upgrade schedule

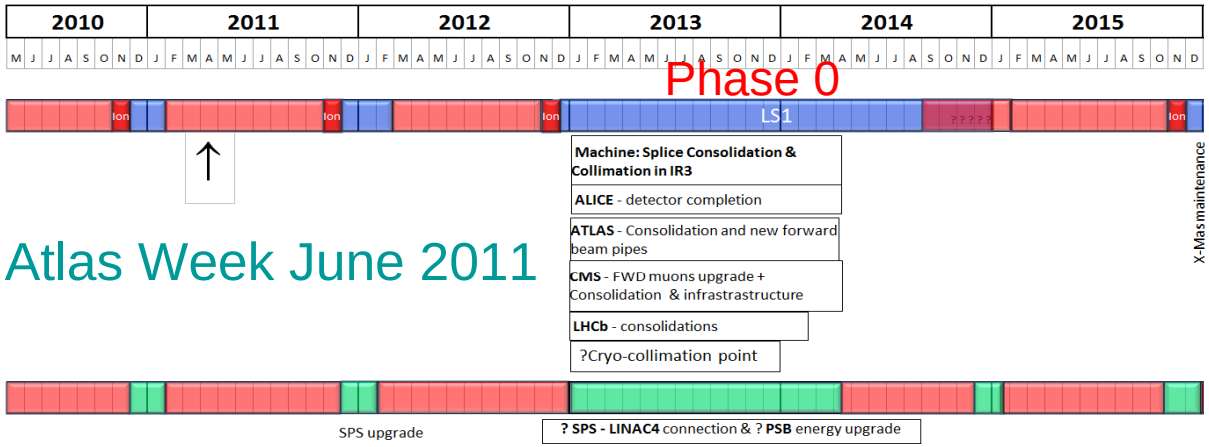
F. Zimmermann, Atlas Week June 2011





Current (not yet approved)upgrade upgrade schedule

New rough draft 10 year plan



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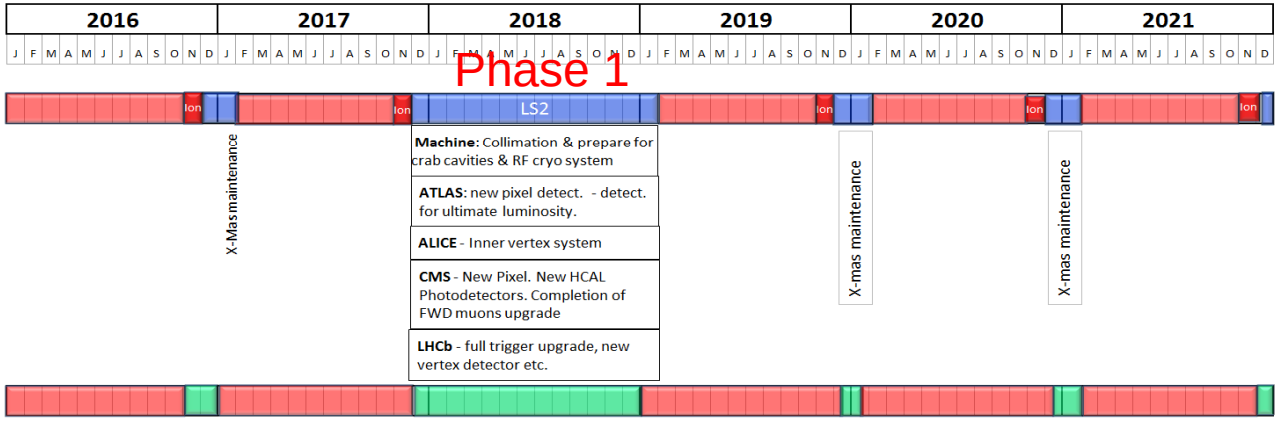


Phase 2

LS3 Installation of sLHC hardware

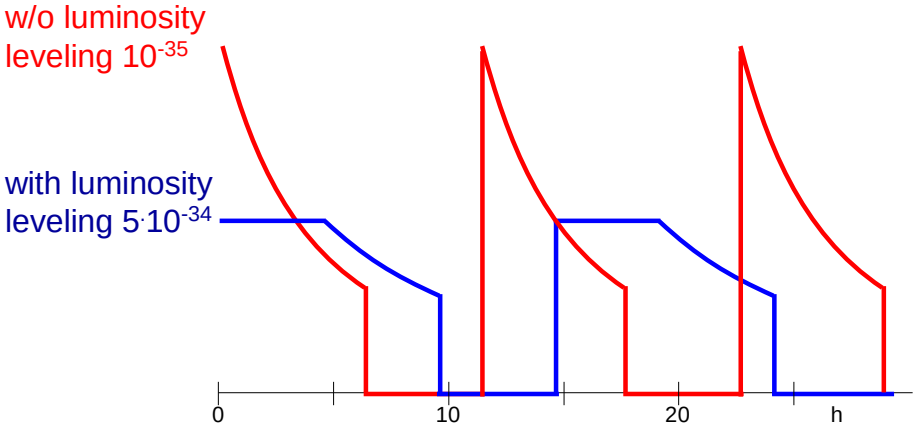
Machine parameter development

Phase 0 – Phase 1: upto $10^{34}cm^{-2}s^{-1}$, initially 6.5+6.5TeV, 25 ns

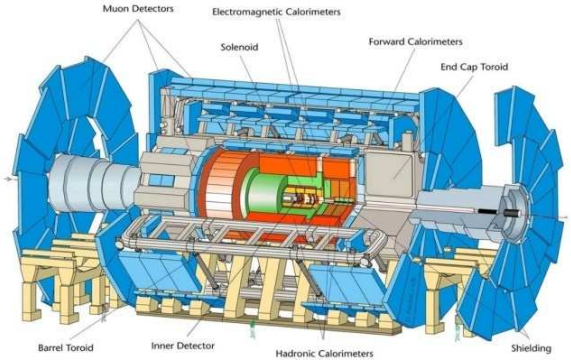
Phase 1 – Phase 2: upto $2\text{-}3 \cdot 10^{34}cm^{-2}s^{-1}$, 7+7TeV, 25 or 50 ns

Phase 2 –: upto $5 \cdot 10^{34}cm^{-2}s^{-1}$, 7+7TeV, 25 or 50 ns, luminosity leveling

Total goal 3000 fb^{-1} by 2030



What are the main issues?



Higher luminosity → more events accepted with current criteria

but level 1 rate stays ~ 100kHz – L2 capacity increased but also event sizes

Higher threshold not the answer → better L1 trigger decisions needed

Better information - Better algorithms – Better architecture

Move down algorithms in trigger hierarchy: EF→L2→L1(→L0)

Higher luminosity → increased occupancy - ~200 minimum bias events/BC → pile up

ID need replacement due to radiation damage and aging

Calorimeter on detector electronics designed for 10 year of $10^{34}cm^{-2}s^{-1}$

FCAL replacement – radiation damage

Fake muon trigger reduction – cavern background – multiple scattering

Phase 0 upgrade

LS 1 (before end 2014)	
Detector consolidation	*Ph0*
L1 improvements (new L1Calo MCMs and CTP core)	*Ph0*
IBL?	*Ph1*
CMX and Phase 0 Topological processor	*Ph1*
LAr and TileCal readout demonstrators	*Ph2*
LS 2 (before end 2018)	
Muon new small wheel + new SL + MuCTPi	*Ph1*
Muon data into L1Topo (or isolation signals into L1Muon?)	*Ph1*
FTK	*Ph1*
Pilot project, new LAr electronics (perhaps more)	*Ph2*
Vertical slice tests for Ph-I and Ph-II	*Ph2*
LS 3 (after 2021)	
LAr and Tilecal new electronics, new Calo Trigger	*Ph2*
Endcap calorimeters	*Ph 2*
New ID, L1 Track Trigger?	*Ph2*
Two-stage trigger (L0/L1)?	*Ph2*
Possible MDT trigger	*Ph2*
Replacement Central Trigger integrated with topo trigger	*Ph2*

Phase where the major upgrade occurs

Phase 1 upgrade

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Detector consolidation	*Ph0*	
L1 improvements(new L1Calo MCMs and CTP core)		*Ph0*
IBL?	*Ph1*	
CMX and Phase 0 Topological processor	*Ph1*	
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Inner Detector Upgrade

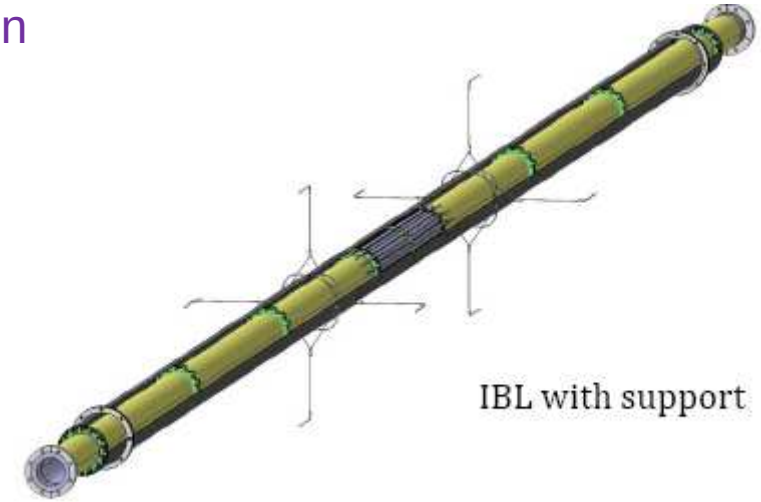
The innermost (B) layer most exposed – need replacement in Phase 1

Old B-layer cannot be removed → New, fourth, B-layer inside at r=33mm
(Insertable B-layer (IBL)) → New smaller Al beam pipe

IBL→ improved performance → Why not in Phase 0 – difficult schedule – may be possible – FE14 (130nm) critical component – planar or 3d - services difficult

CO_2 evaporative cooling using Ti pipes, Carbon fibers to make mechanical structure strong and thin

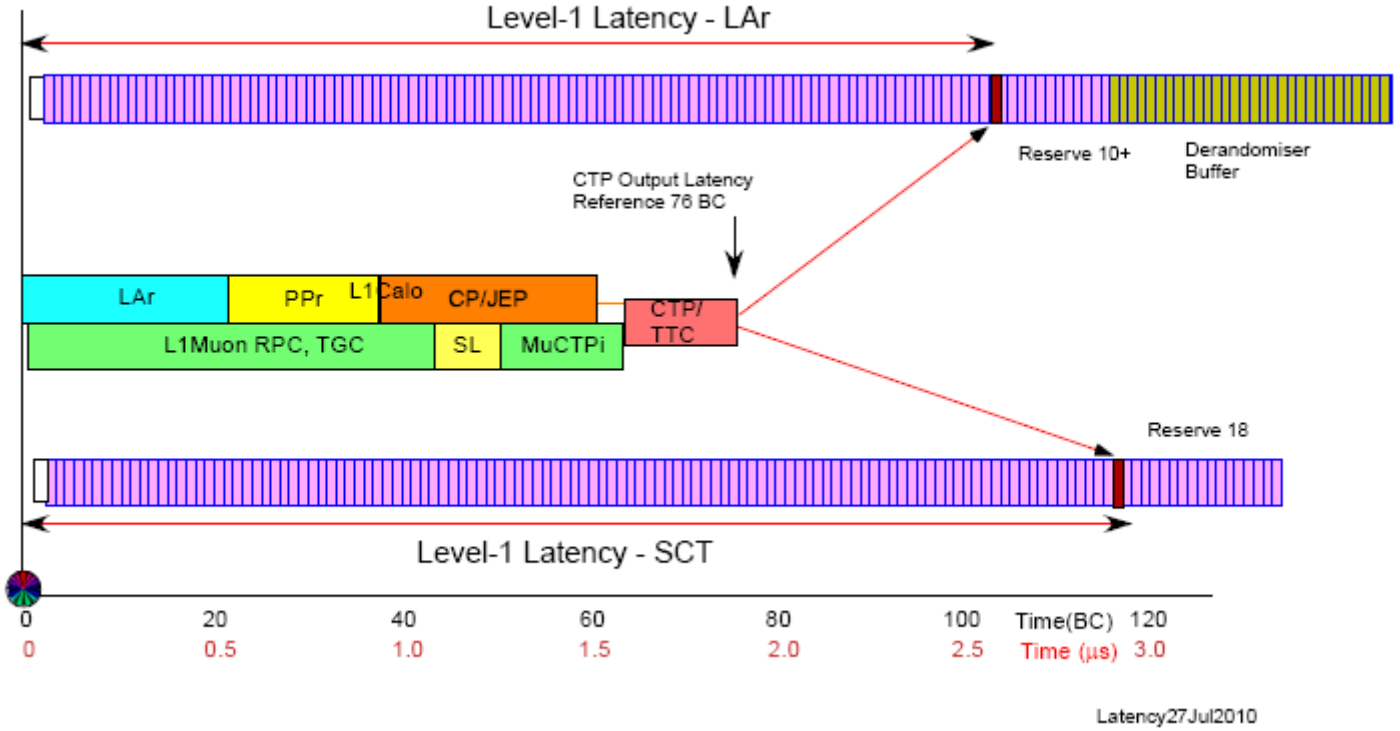
160 Mb/s optical links



Picture from R. Beccherle, ACES

TDAQ Phase 1 Upgrade

Add new functionalities → Longer latencies – must fit in available latency budget (Norman Gee)



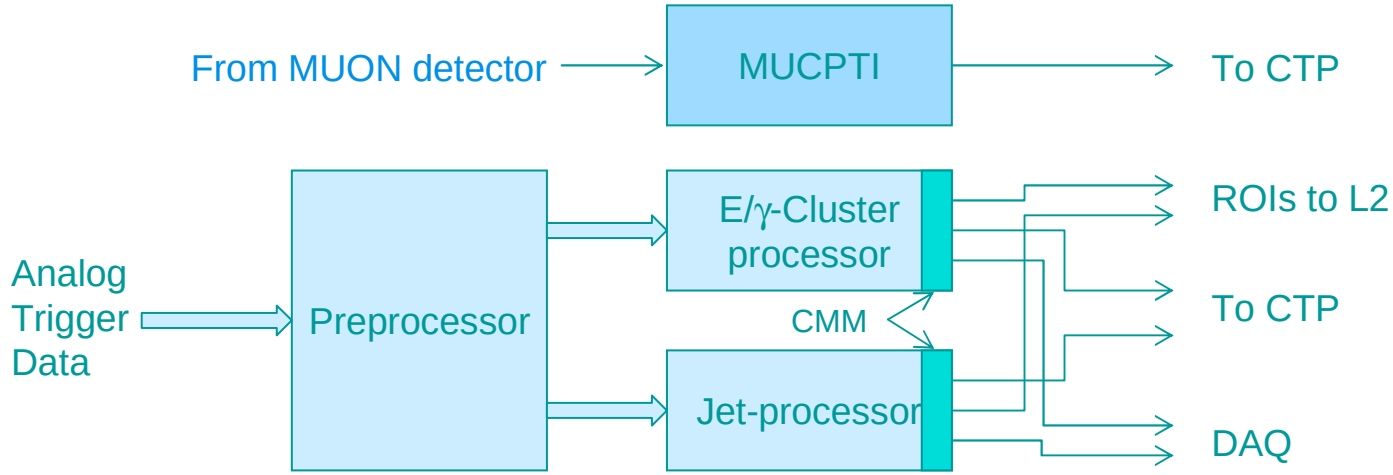
TDAQ Phase 1 Upgrade

Potential latency consumers:

- New MCM + new CTP core
- Topological L1 trigger
- New Small Muon Wheel
- (Digital Full readout of calorimeter data)

Topological L1 Trigger

The present calorimeter trigger reports number of different events to CTP and their positions (ROIs) to Level 2



Find and report # em, tau (energies) and jet (size and energy) objects passing limited # of thresholds

Report global Missing ET (MET) and Sum ET

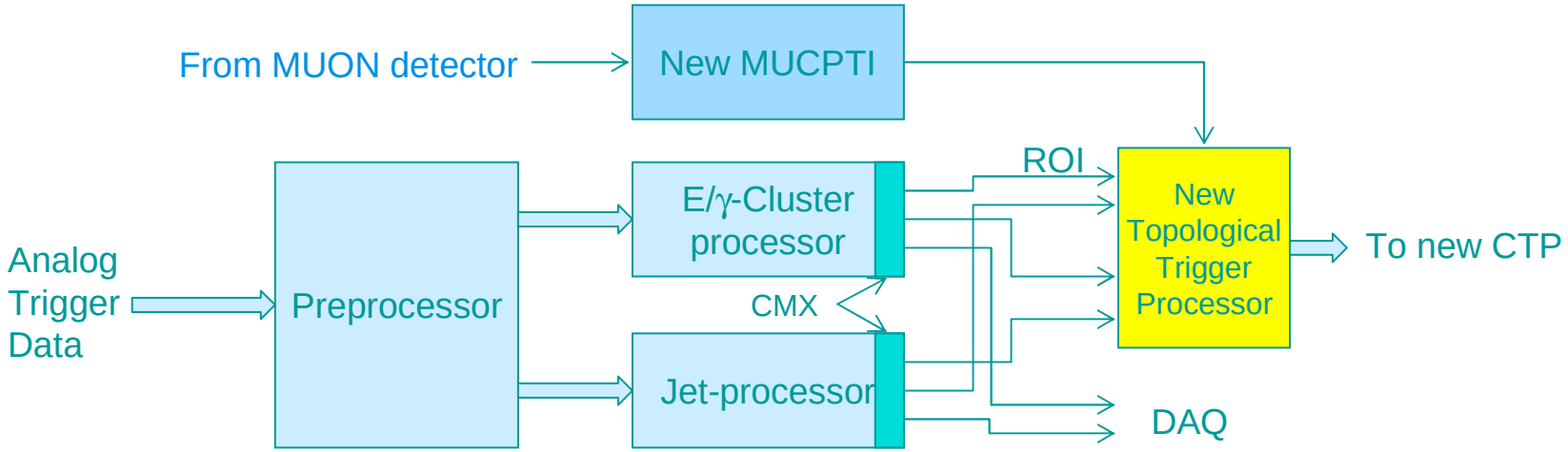
Report positions (ROIs) to L2

However, positions are not used at L1

CMM = Common Merger Module

Topological L1 Trigger

By combining the number of different events and ROIs in a topological processor



Directional correlations are made available to the CTP and ambiguous events may be resolved

Reprogram cluster and jet processor boards so that they send ROIs over the backplane (at 4x speed) to the modified CMXs

CMX eXtended Comman Merger module

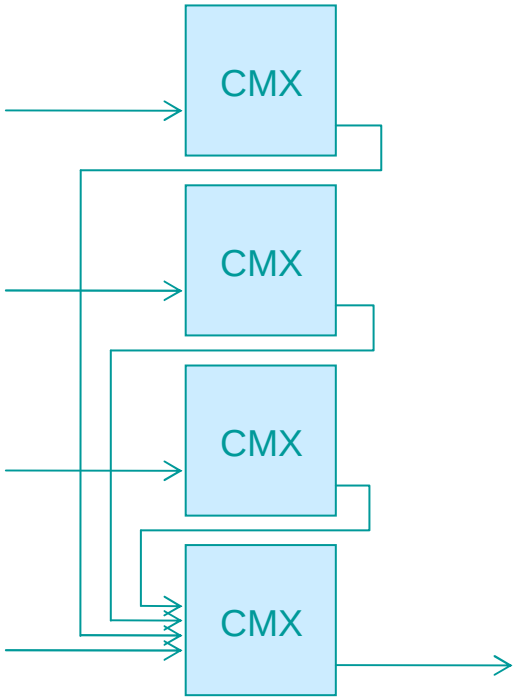
Topological L1 Trigger

After the upgrade a range of topological triggers are available:

Overlap removal em, jets
$\Delta\phi$
$\Delta\eta$
R — Angular distance
Back to back
Not back to back
M — Reconstructed mass

Topological L1 Trigger

The CMX contains processing elements (FPGAs) and extra high speed links, which allows some topological processing in case of topo module production problems



The CMX will be installed in first long shutdown (LS1) along with a Topo demonstrator
An expanded Topo function will be installed in LS2

Muon detector problems

Some muon trigger levels will saturate the trigger with fakes
Fakes may be caused by false coincidences with cavern background (neutrons) or tails from previous BC
New beam pipe will reduce cavern background (~30% reduction of fakes)
Improved shielding will also help

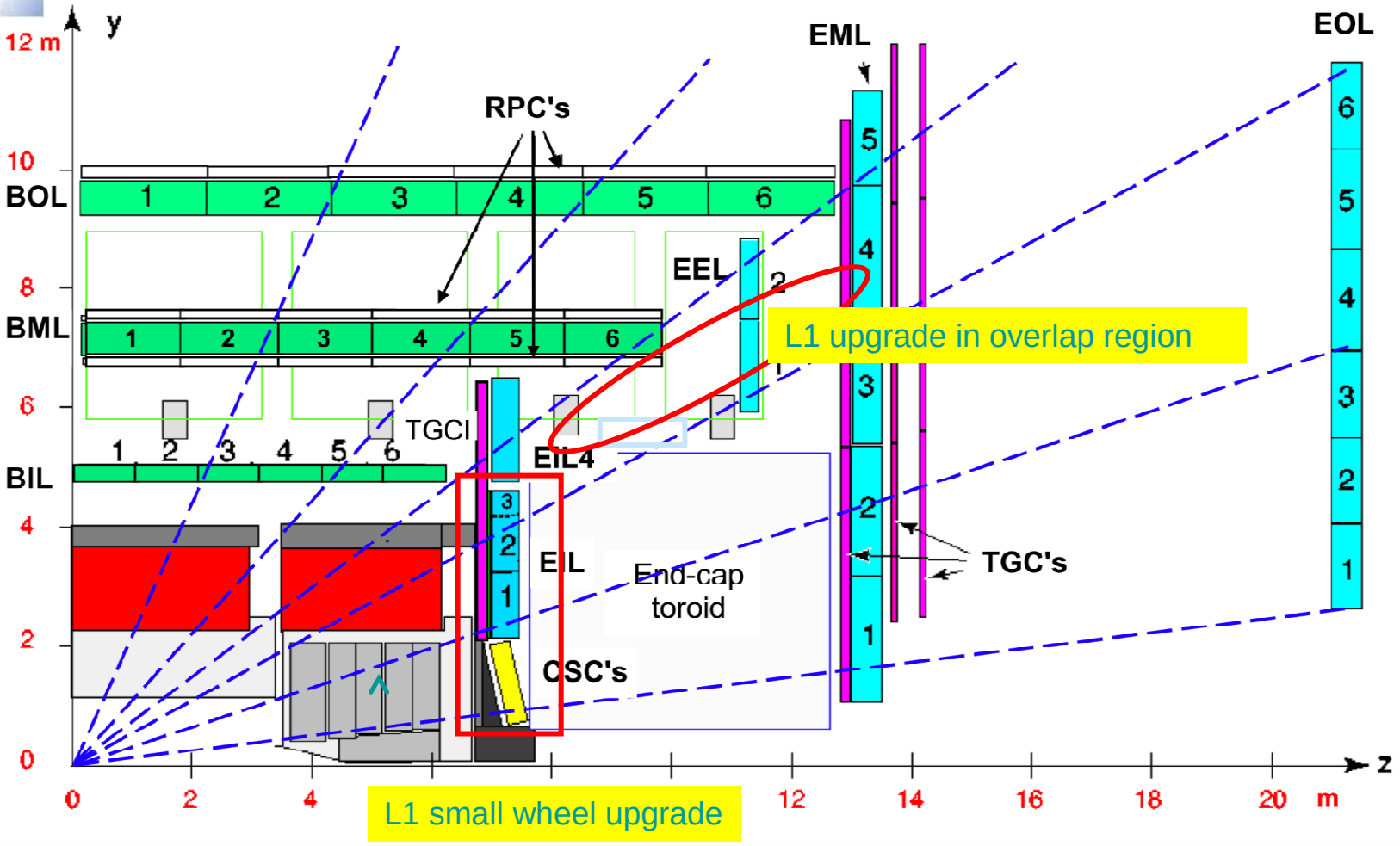
Multiple scattering problem

Muon isolation

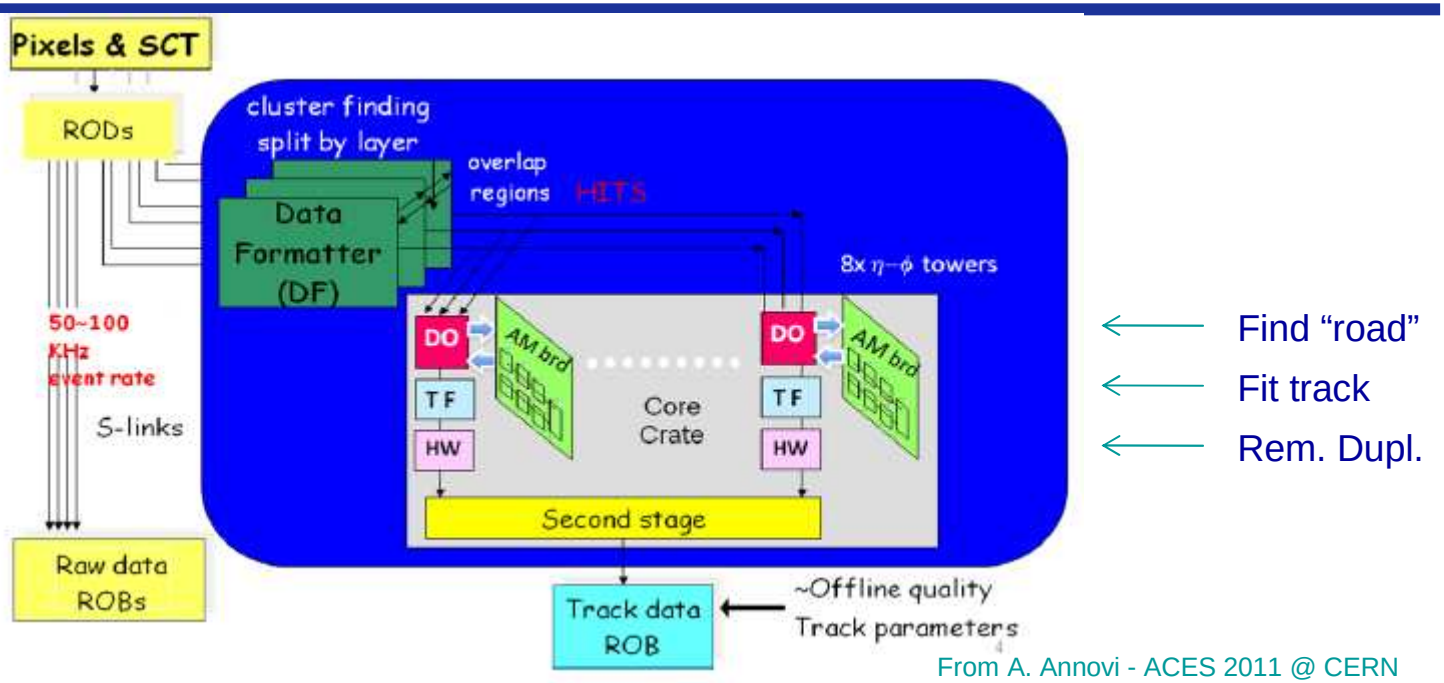
A new small wheel, which will improve momentum and directional resolution (1 mrad) will sharpen thresholds and removes fakes in the endcap region

Technology choice still open. The following options are considered:
Thin MDT
New TGC
MicroMegas

Small wheel upgrade



FTK



From A. Annovi - ACES 2011 @ CERN

Aim - global track reconstruction by the start of level-2 trigger (CDF)

The FTK's dual path RODs decouples from standard operation

Use 8 planes initially

Cluster finding send hits - Find pattern among AMs 10^9 stored patterns – Fit track – remove duplications - use all planes

Barrel 2014, rest later – extensive simulations

Fast 25µs @ $3 \cdot 10^{34}$ – finds tracks with almost off line precision

Phase 2 upgrade

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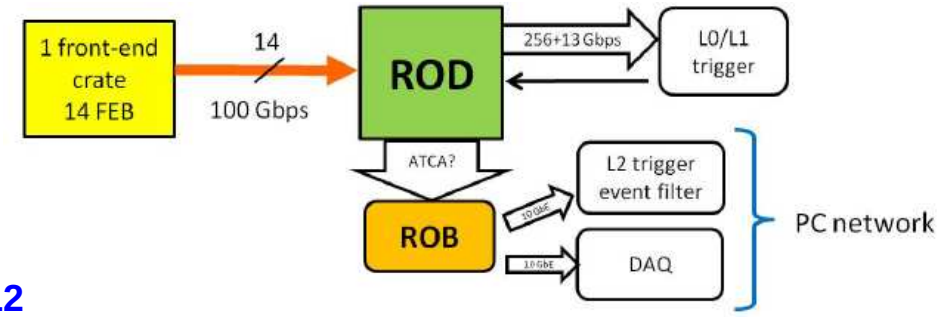
LAr Phase 2 Upgrade

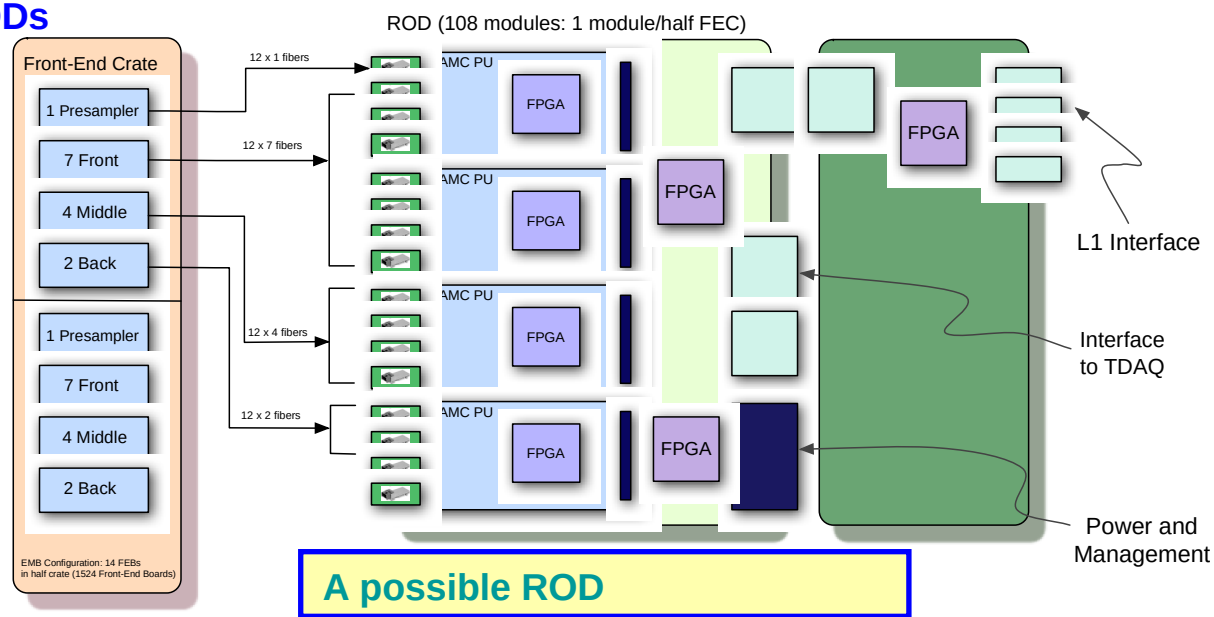


Full digital readout of all data to USA-15

Data bandwidth of entire LAr w. 1524 FEBs > 150Tbps (no redundancy)

- **High speed parallel fiber optical transceiver (e.g. 12 fibers @ 10Gbps)**
- **The are upgrade R&D projects for developing high speed links, ADC solutions and RODs**

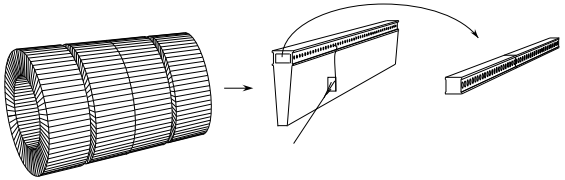
Trigger access to full LAr resolution



A possible ROD implementation

Based on slide from Hucheng Chen

TileCal Phase 2 Upgrade



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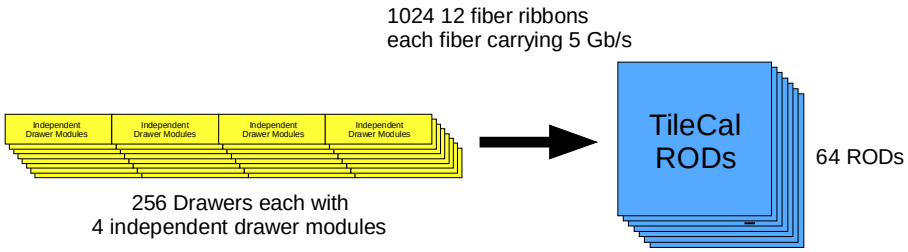
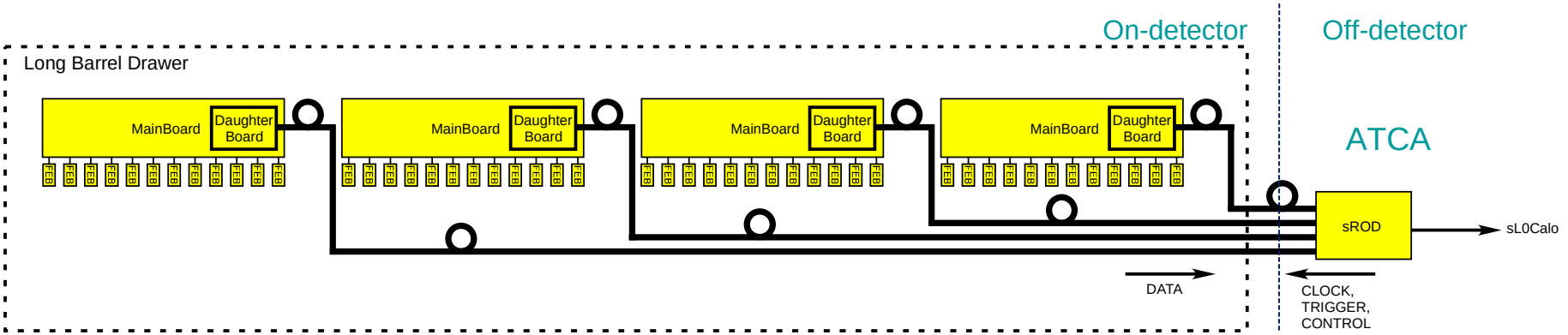


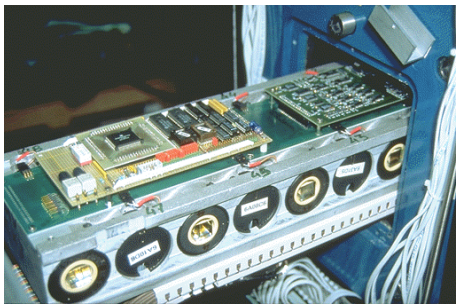
- **Data bandwidth of entire TileCal with 1024 independent drawer modules --> 50Tbps with duplication for redundancy**
  - **High speed 5Gb/s optical fibers**



The main components of an upgraded drawer are:

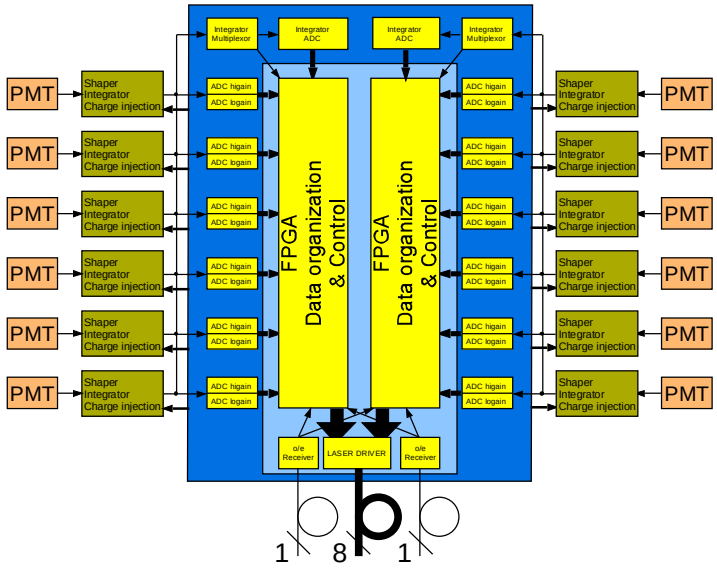
- New front-End boards – three alternative designs (3-in-1, FE-ASIC, QIE)
- MainBoards – digitizing the FE signals
- Processing Daughter Board – processing and high speed communication
- New PMT dividers – new HVPS – new LVPS

Off detector - sROD modules



TileCal Phase 2 Upgrade

Drawer Readout



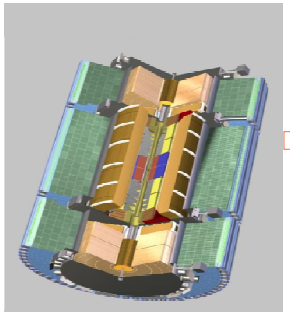
- 4-fold redundancy – all fibers duplicated and 2 channels (on different fibers) per cell
- Clock, Trigger and Control are obtained via the GBT protocol
- Early prototypes are being developed
- FPGA radiation tolerance must be verified

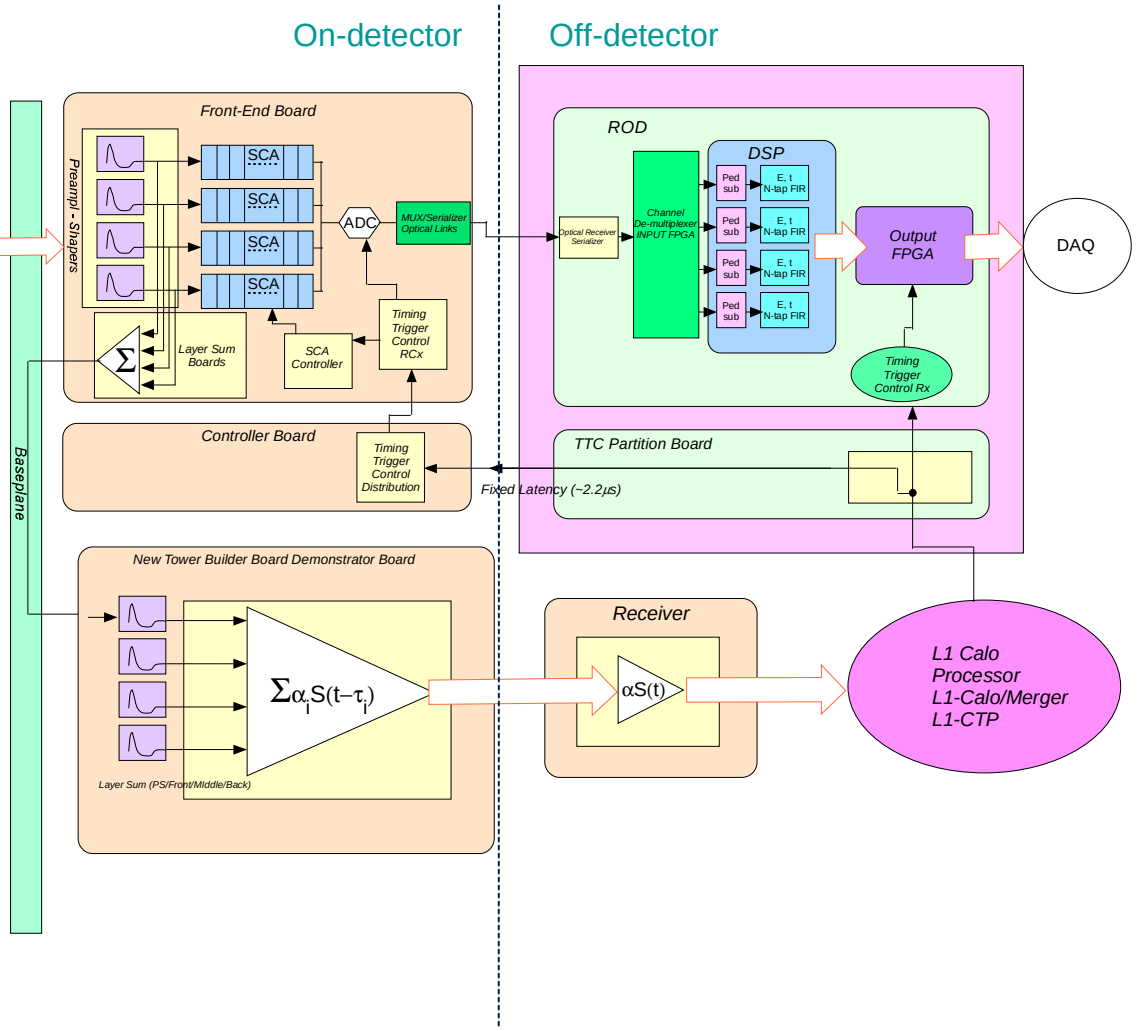
The Calorimeter Readout Demonstrator Project

The Demonstrator project aims at a coordinated yet independent installation of digital trigger data links in a limited area (.4x.4) of both LAr and TileCal during LS1.

The new data path should operate in parallel with present analog trigger data path thus be compatible with the present trigger and readout

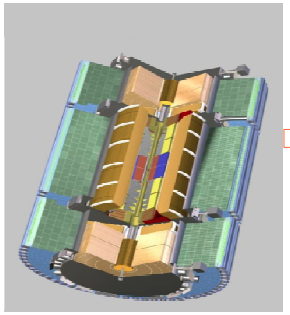
Current LAr Architecture





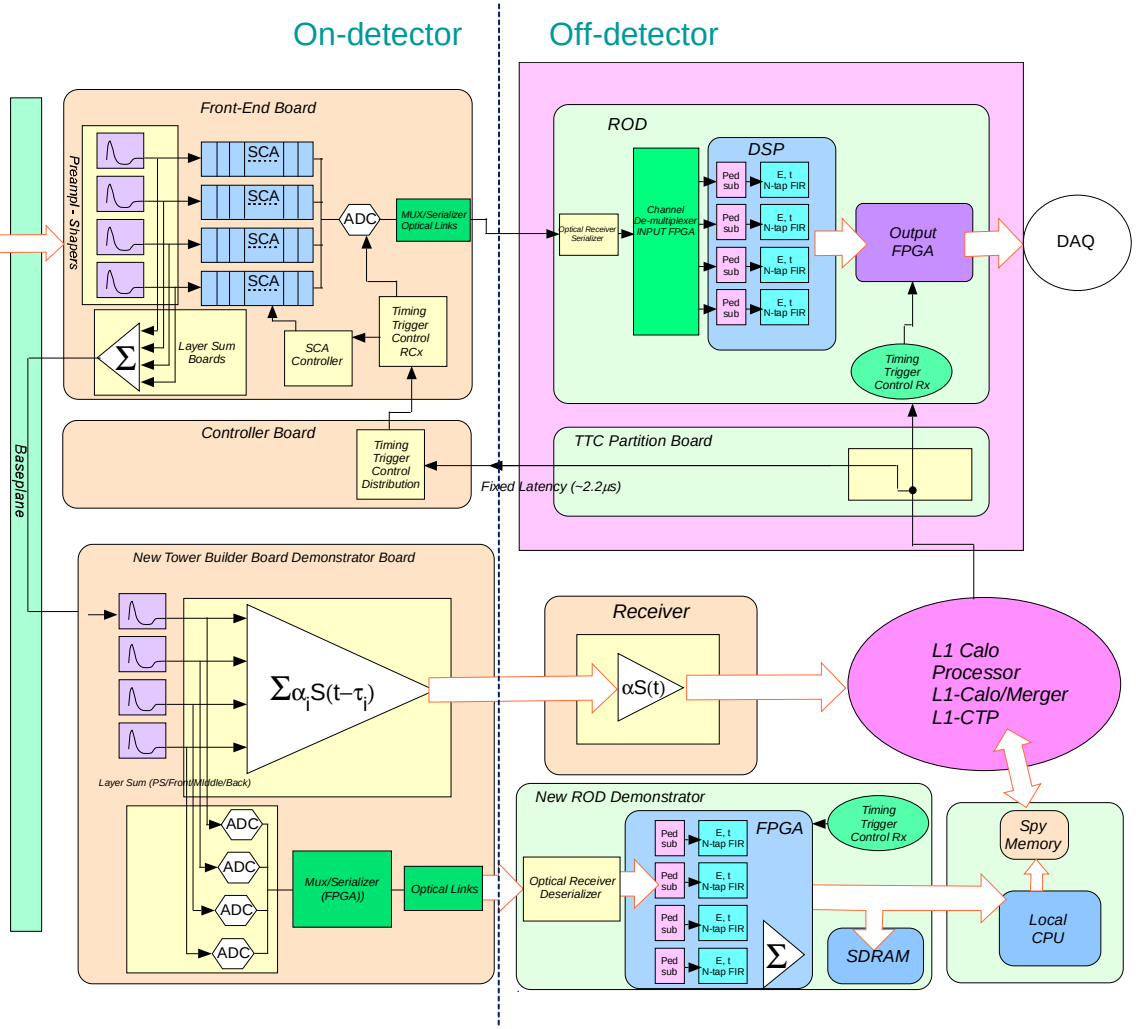
- **Analog trigger tower signals sent to L1Calo through TBB and Receiver, digitization happens on Pre-processor**

Slide from F.Lanni



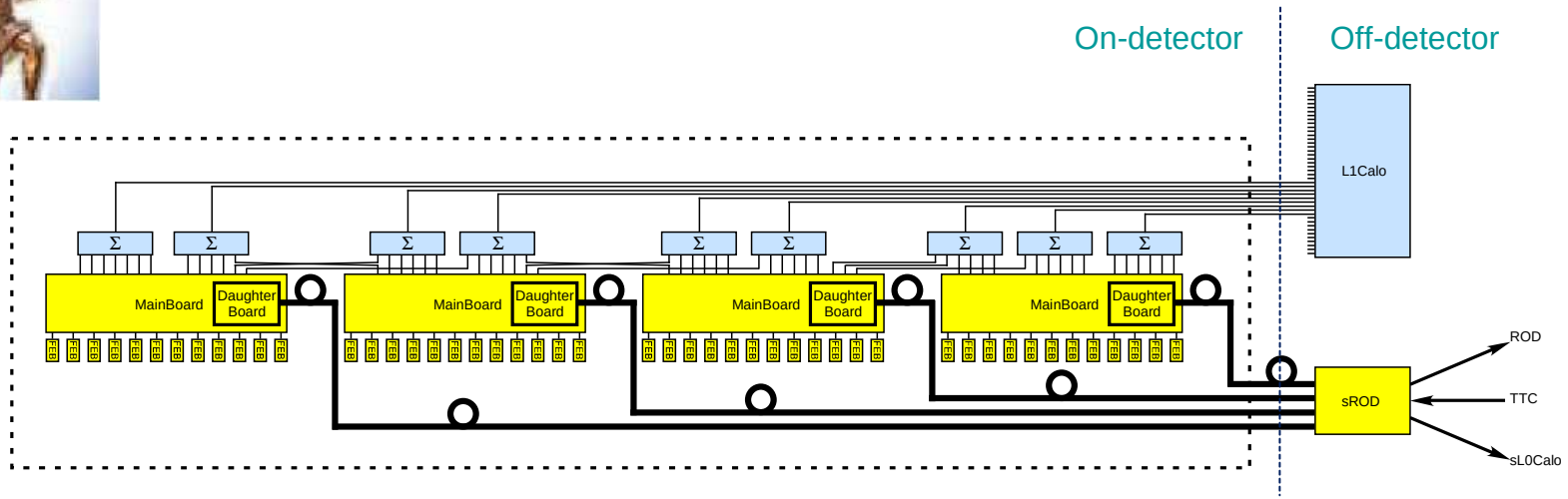
Idea for LAr Demonstrator System

- **Phase 0: ~3k channels max, 0.4x0.4 are on one side of the barrel calorimeter**
- **Phase-1: extend to the full calorimeter trigger readout (~20k channels max), L1 trigger potentially using digitized layers**



Slide from F.Lanni

A TileCal hybrid drawer design

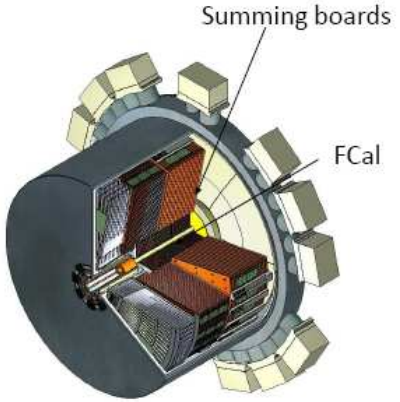


The plan is to develop a hybrid demonstrator drawer compatible with the present system aiming at evaluation in TileCal test facilities before the end of 2013 and then insertion of one hybrid drawer in ATLAS in the end of LS1

Providing analog readout via present summation boards

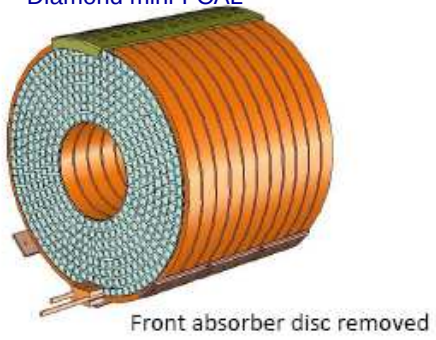
Firmware in the sROD module interfaces the TTC inputs and the ROD outputs

FCAL Upgrade



Loss of efficiency in FCAL at High Luminosities
Excessive HV drop and space charge effects
Solutions:
1: New improved sFCAL new electronics and improved cooling → open cryostat and long shutdown
2. Warm mini FCAL in front of FCAL
A: Using Diamond detector – Could be installed in Ph 1
B: Similar to FCAL but using high pressure Xe

Diamond mini-FCAL



From G.Oakham AUW Oxford March 2011

Track Trigger

One way to reduce the fake muons is to correlate them with a track in the ID at L1.
A track trigger would also improve electron selection at L1
Whether a track trigger is necessary is being evaluated with simulations.

A L1 track trigger can be made in two ways:

Self seeded – reports high p_T tracks

need fast communication to form coincidences between layers – difficult – requires complete redesign of tracker – might operate w latency of ~3μs

ROI seeded – less redesign of tracker but, needs a L0 trigger to provide ROIs and long ~10μs L1 latency

A hi res Track Trigger might even provide impact parameters → L1 b-trigger

The track trigger would be incuded in the new ID that will be installed in Phase 2

Inner Detector Upgrade

The TRT will be removed in Phase 2
Different new ID layouts studied – larger size – larger pixel, larger strip - Utopia project

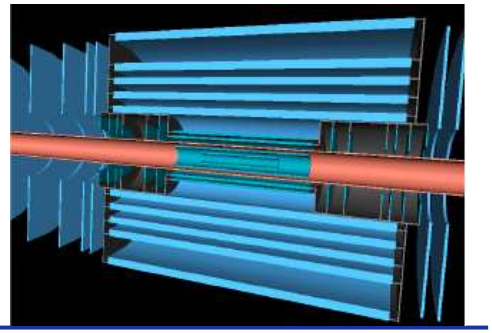
The new inner detector parts are designed with smaller feature sizes – 65nm planar
or new 3d-technologies
Smaller feature sizes →
more tolerant to permanent errors, but more sensitive to transient errors
High speed optical links based on redundant data protocols (GBT*) and Versatile link*

Improved services – less material, less power dissipation, better cooling, better power supplies (serial power or DC-DC)
Smaller detector features – better resolution – reduced occupancy

Upgrade ID together in Ph 2 or Pixel already in Ph 1. Can
Pixel last for 12 years – unlikely – more LS - more upgrades

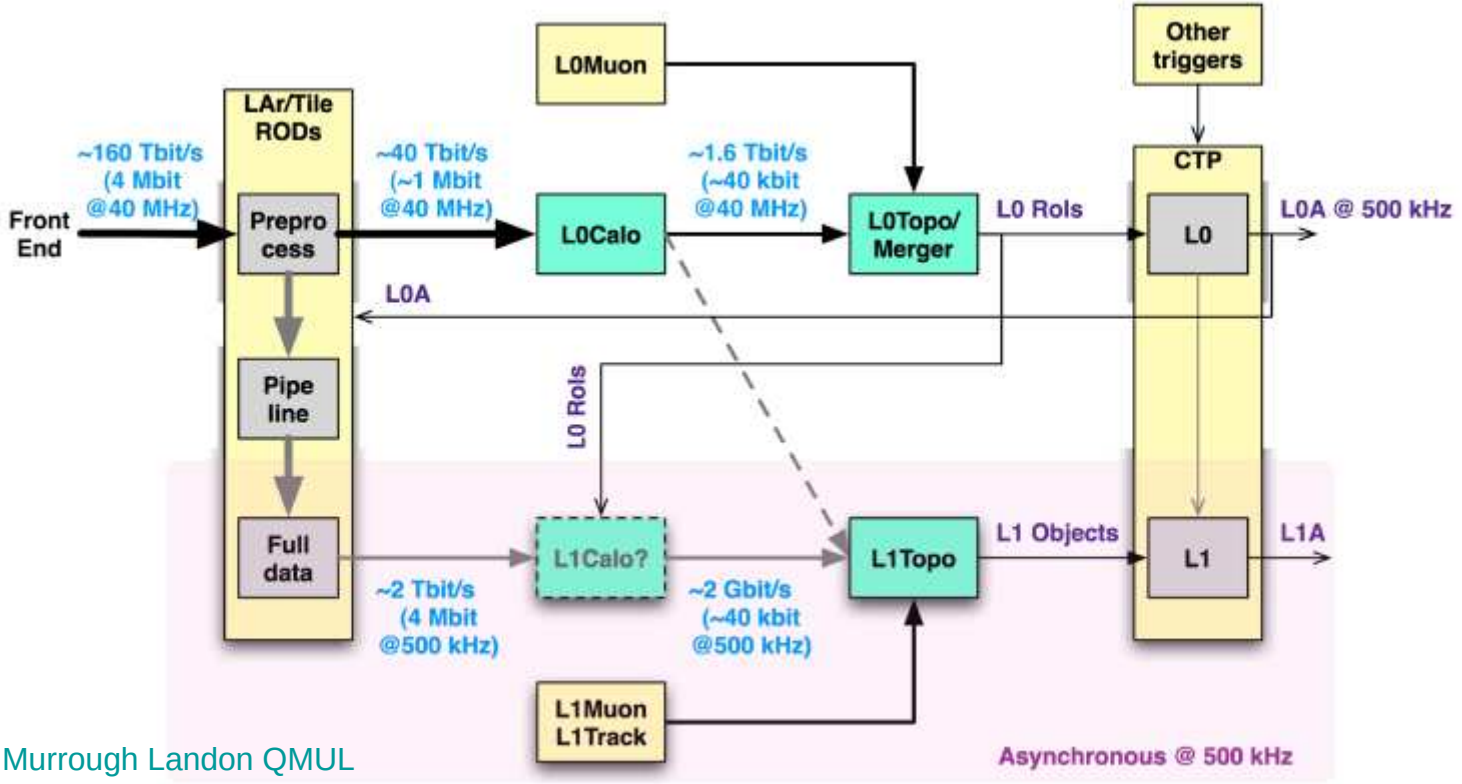
Pixel: experience from IBL, develop RO-chip FE-I4 (pixel)
SCT: RO-chip ABCDN-13 IN 130 nm

* CERN R&D development projects



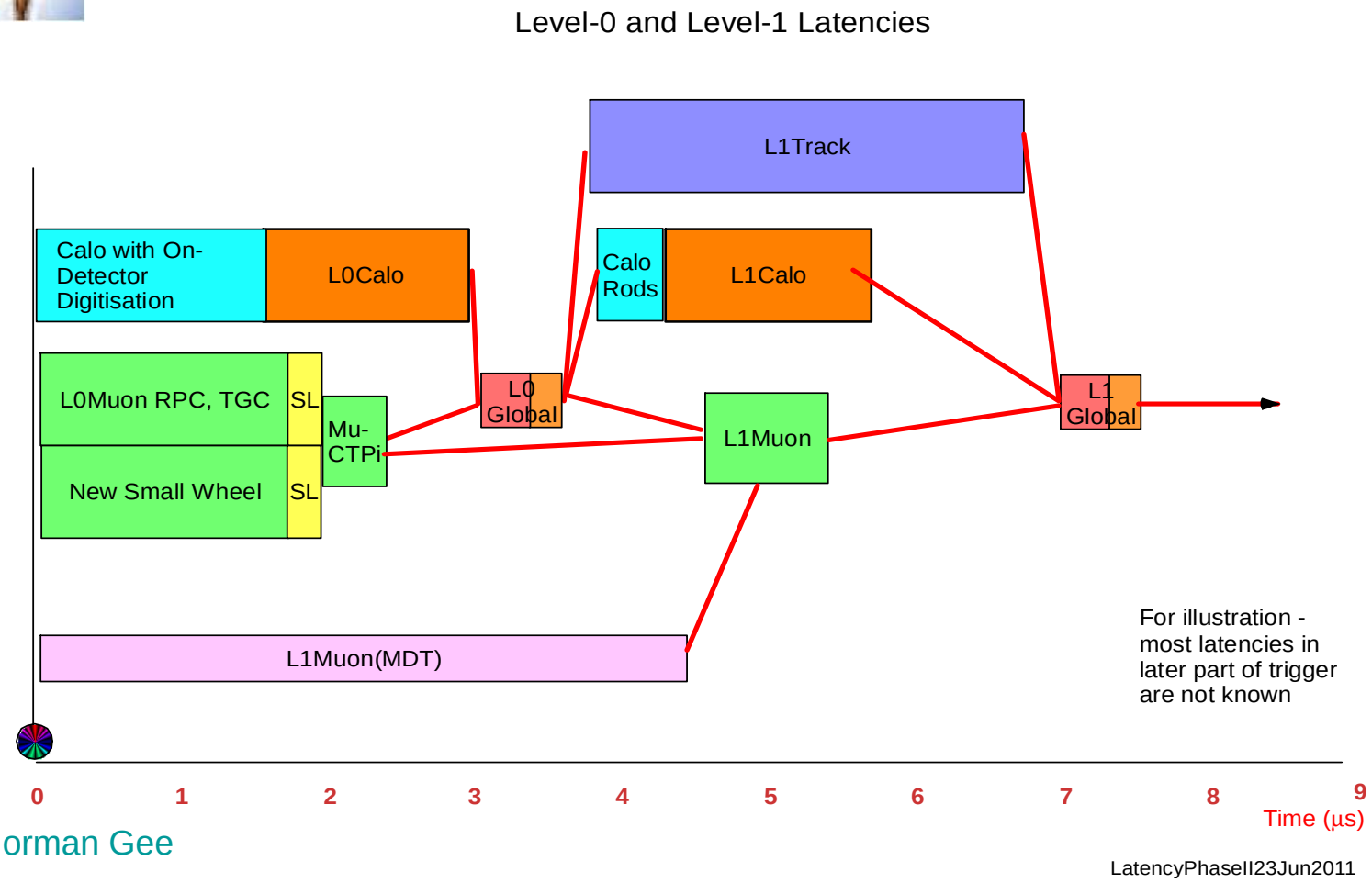
Two stage trigger (L0/L1)

A ROI driven trigger needs a L0 trigger to provide ROIs



Murrough Landon QMUL

Phase-II – approx. timing sequence



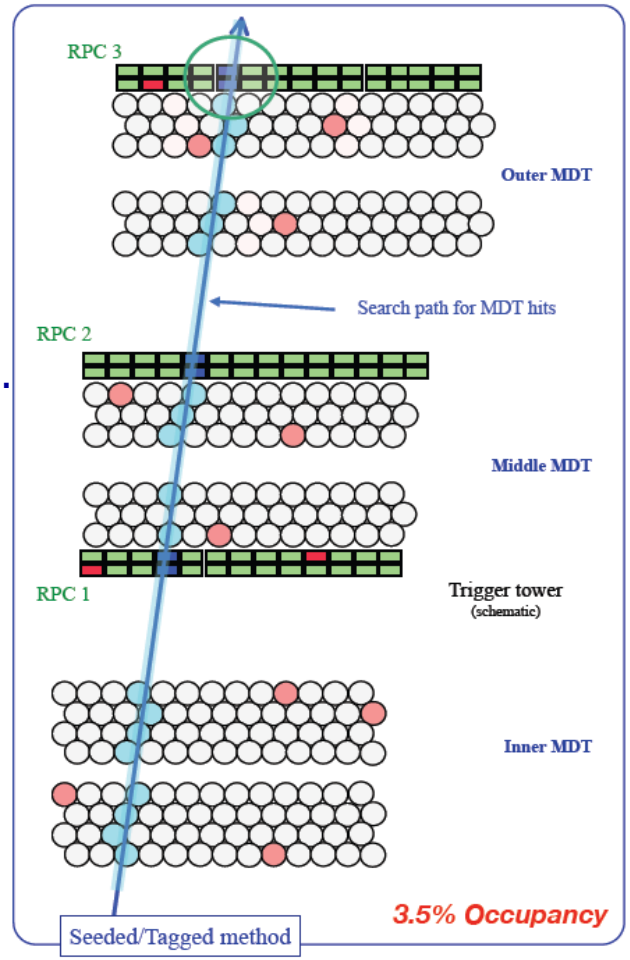
Slide: Norman Gee

LatencyPhaseII23Jun2011

Possible Phase 2 Muon Upgrades

Use MDTs to improve the trigger p_T resolution.

MDTs are slow and precise (100 times that of RPC),
The long Phase 2 latency allow a precision 10 times RPC.
using RPC seeded data



D della Volpe, L1 Upgrade meeting Stockholm 2011

Summary

There are many suggestions about how to improve the detector performance and sometimes many alternatives for each action.

These are being evaluated and compared using simulations and test (beam) results.

The final choices will all have to be installed during limited shut down periods available causing considerable logistic difficulties

The phase 1 upgrade program is taking shape and a phase 1 upgrade LoI is under development to be submitted at the end of the year.

Phase 2 is converging